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EXAMINER	
YIGDALL, MICHAEL J	
ART UNIT	**PAPER NUMBER**
2122	

DATE MAILED: 01/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/044,690	WILKERSON ET AL.	
	Examiner	Art Unit	
	Michael J. Yigdall	2122	

-- The MAILING DATE of this communication appears on the cov r sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892).
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/10/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-29 are pending and have been examined. The priority date considered for the application is January 9, 2002.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-5, 14-18, 21-24, 27 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over "Value Speculation Scheduling for High Performance Processors" by Fu et al. (hereinafter "Fu").

With respect to claim 1, Fu discloses a method comprising:

(a) creating a data flow graph associated with a program (see, for example, page 266, Figure 7, step 3, which shows creating a data dependence or data flow graph);

(b) identifying a first instruction that is to be executed after a second instruction (see, for example, page 263, column 2, lines 1-3 and Figure 3(a), which shows an instruction I4, i.e. a first instruction, that is to be executed after an instruction I3, i.e. a second instruction);

(c) determining that an outcome of the first instruction is dependent on an outcome of the second instruction based on the data flow graph (see, for example, page 263, column 2, lines 7-9

and page 264, Figure 4(a), which shows that an outcome of the first instruction I4 is dependent on an outcome of the second instruction I3).

Although Fu does not expressly disclose the limitation wherein the outcome of the second instruction represents a key into a software structure that includes a set of keys and a corresponding set of predicted outcomes of the first instruction, Fu does, however, disclose a table of predicted values in which each entry in the table has an index or key (see, for example, page 264, column 1, lines 29-33). The values in the table represent predicted operands of the first instruction I4, based on predicted outcomes of the second instruction I3, and enable the first instruction I4 to be speculated (see, for example, page 264, column 1, lines 6-13).

It would have been apparent one of ordinary skill in the art at the time the invention was made that the index or key into the table disclosed by Fu could be designated as the outcome of the second instruction, or any such value, so long as unnecessary conflicts are avoided (see, for example, page 264, column 1, lines 29-33).

Fu also discloses:

(d) inserting a third instruction to be executed after the second instruction and before the first instruction (see, for example, page 263, Figure 3(b), which shows inserting an instruction I7, i.e. a third instruction, after the second instruction I3 and before the first instruction I4), wherein the third instruction is to retrieve a predicted outcome of the first instruction from the software structure based on the outcome of the second instruction (see, for example, page 264, column 1, lines 10-15, which shows that the third instruction I7 retrieves a predicted value from the table).

With respect to claim 2, Fu also discloses the limitation wherein the second instruction precedes the first instruction during the execution of the program by one or more intermediate

instructions (see, for example, page 263, Figure 3(a) and page 264, Figure 4(a), which shows that a second instruction such as I1, an instruction on which the first instruction I4 depends, may precede the first instruction I4 by one or more intermediate instructions).

With respect to claim 3, Fu also discloses the limitation wherein the software structure is a lookup table (see, for example, page 264, column 1, lines 29-33, which shows an indexed table, i.e. a lookup table).

With respect to claim 4, Fu also discloses the limitation wherein each predicted outcome in the software structure is an outcome resulted from a last execution of the first instruction when an outcome of the second instruction was equal to a key associated with said each predicted outcome in the software structure (see, for example, page 265, column 1, lines 16-18, which shows that the predicted value is the last value, i.e. an outcome resulted from the last execution).

With respect to claim 5, Fu also discloses:

(a) inserting a fourth instruction to be executed after the first instruction (see, for example, page 263, Figure 3(b), which shows inserting an instruction I9, i.e. a fourth instruction, after the first instruction I4), the fourth instruction is to update the software structure with the value resulted from the execution of the first instruction with the corresponding outcome of the second instruction (see, for example, page 264, column 1, lines 15-18, which shows that the fourth instruction I9 updates the table with the resulting value).

With respect to claim 14, the apparatus recited in the claim corresponds to the method recited in claim 1 (therefore, see Fu as applied to claim 1 above). Note that Fu also discloses a compiler (see, for example, page 267, column 2, lines 8-18).

With respect to claims 15-18, the limitations recited in the claims are analogous to the limitations recited in claims 2-5, respectively (therefore, see Fu as applied to claims 2-5 above, respectively).

With respect to claim 21, the system recited in the claim corresponds to the method recited in claim 1 (therefore, see Fu as applied to claim 1 above). Note that Fu also discloses a compiler (see, for example, page 267, column 2, lines 8-18). A memory and a processor are inherently provided to store and execute the compiler, respectively, without which the prediction method of Fu would be inoperative.

With respect to claims 22-24, the limitations recited in the claims are analogous to the limitations recited in claims 2, 4 and 5, respectively (therefore, see Fu as applied to claims 2, 4 and 5 above, respectively).

With respect to claim 27, the computer readable medium recited in the claim corresponds to the method recited in claim 1 (therefore, see Fu as applied to claim 1 above).

With respect to claim 28, the limitations recited in the claim are analogous to the limitations recited in claim 2 (therefore, see Fu as applied to claim 2 above).

4. Claims 6-9, 19, 25 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fu, as applied to claims 1, 14, 21 and 27 above, respectively, in view of U.S. Pat. No. 6,308,322 to Serocki et al. (hereinafter "Serocki").

With respect to claim 6, Fu does not expressly disclose the limitation wherein the first instruction is a branch instruction.

However, Serocki discloses predicting the outcomes of branch instructions so as to increase processing speed (see, for example, column 4, lines 15-17). Serocki discloses that the invention is not limited to any particular method of prediction (see, for example, column 7, lines 30-35, and column 8, lines 7-12).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the prediction method of Fu to predict the outcomes of branch instructions, and accordingly increase processing speed, as taught by Serocki.

With respect to claim 7, Serocki further discloses the limitation wherein the branch instruction is any one of an indirect branch instruction and a direct branch instruction (see, for example, column 4, lines 28-42, which shows that the branch instructions are indirect branches).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the prediction method of Fu to predict the outcomes of indirect branch instructions, and accordingly increase processing speed, as taught by Serocki.

With respect to claim 8, Fu also discloses the limitation wherein the outcome of the second instruction is a value that determines the outcome of the first instruction (see, for

example, page 263, Figure 3(a), which shows that the outcome of the second instruction I3 is a value, stored in R4, that determines the outcome of the first instruction I4).

With respect to claim 9, Fu also discloses the limitation wherein the outcome of the second instruction is a data address of a value that determines the outcome of the first instruction (see, for example, page 263, Figure 3(a), which shows that the outcome of a second instruction I2 is a data address of a value, subsequently stored in R4 by instruction I3, that determines the outcome of the first instruction I4).

With respect to claim 19, the limitations recited in the claim are analogous to the limitations recited in claim 6 (therefore, see Fu and Serocki as applied to claim 6 above).

With respect to claim 25, the limitations recited in the claim are analogous to the limitations recited in claim 6 (therefore, see Fu and Serocki as applied to claim 6 above).

With respect to claim 29, the limitations recited in the claim are analogous to the limitations recited in claim 6 (therefore, see Fu and Serocki as applied to claim 6 above).

5. Claim 10-13, 20 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fu, as applied to claims 1, 14 and 21 above, respectively, in view of U.S. Pat. No. 6,687,807 to Damron (hereinafter "Damron").

With respect to claim 10, Fu does not expressly disclose the limitation wherein the first instruction is a linked list instruction.

However, Damron discloses efficiently generating prefetch instructions for pointer-based data structures (see, for example, column 2, lines 43-48), such as linked lists (see, for example, column 2, lines 12-15), so as to mitigate memory latency problems (see, for example, column 2, lines 2-5). Damron discloses that the additional memory hardware of the invention is relatively small and provides the CPU with relatively fast access (see, for example, column 2, lines 62-67).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement the prediction method of Fu with the prefetching and linked list features taught by Damron, so as to predict the outcomes of linked list instructions, and accordingly mitigate the memory latency problems associated such pointer-based data structures.

With respect to claim 11, Fu also discloses the limitations wherein:

(a) each key in the software structure is a pointer to a producer item in a linked list (see, for example, page 264, column 1, lines 29-33 and page 266, column 2, lines 30-34, which shows that the index or key in the table corresponds or points to an instruction selected for value prediction, i.e. a producer instruction, such as a producer item in a linked list); and

(b) a predicted outcome corresponding to said each key in the software structure is a predicted pointer to a target item in the linked list (see, for example, page 263, Figure 3(a), which shows that the outcome of an instruction I2 is a data address of a target value, i.e. a pointer to a target value, such as a pointer to a target item in the linked list);

(c) wherein the producer item precedes the target item in the linked list by one or more intermediate items (see, for example, page 263, Figure 3(a) and page 264, Figure 4(a), which shows that an instruction such as a producer item may precede an instruction such as a target item by one or more intermediate instructions).

With respect to claim 12, Fu also discloses the limitations wherein:

(a) the third instruction is to retrieve the predicted pointer of the target item from the software structure (see, for example, page 264, column 1, lines 14-15, which shows that the third instruction I7 retrieves the predicted value from the table); and

(b) the third instruction is to be executed in parallel with one or more instructions that obtain pointers to the one or more intermediate items (see, for example, page 263, column 2, lines 14-18 and page 264, Figure 4(b), which shows that the third instruction I7 is executed in parallel).

With respect to claim 13, Fu also discloses the limitations wherein:

(a) each key in the software structure is a value of a producer item in a linked list (see, for example, page 264, column 1, lines 29-33 and page 266, column 2, lines 30-34, which shows that the index or key in the table is a value corresponding to an instruction selected for value prediction, i.e. a producer instruction, such as a producer item in a linked list); and

(b) a predicted outcome corresponding to said each key in the software structure is a predicted value of a target item in the linked list (see, for example, page 263, Figure 3(a), which shows that the outcome of an instruction I3 is a target value, such as a value of target item in the linked list);

(c) wherein the producer item precedes the target item in the linked list by at least one intermediate item (see, for example, page 263, Figure 3(a) and page 264, Figure 4(a), which shows that an instruction such as a producer item may precede an instruction such as a target item by at least one intermediate instruction).

With respect to claim 20, the limitations recited in the claim are analogous to the limitations recited in claim 10 (therefore, see Fu and Damron as applied to claim 10 above).

With respect to claim 26, the limitations recited in the claim are analogous to the limitations recited in claim 10 (therefore, see Fu and Damron as applied to claim 10 above).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael J. Yigdall whose telephone number is (571) 272-3707. The examiner can normally be reached on Monday through Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (571) 272-3695. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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